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A sustainable power architecture for mobile computing systems

Ali Muhtaroglu [a,1], Alex Yokochi [b,*], Annette von Jouanne [a]

[a] School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331-5501, USA
[b] School of Chemical, Biological and Environmental Engineering, Oregon State University, Corvallis, OR 97331-2702, USA

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Abstract

Extension of battery life and dissipation of heat from components with high power density are significant challenges in mobile computing platforms. A power architecture suitable for the integration of low voltage, low power renewables into the bus is described in this paper as an innovative, green approach to help both of these issues. The architecture is both scaleable and flexible in order to accommodate the intermittent nature of the renewable energy sources. A new charge pump based boost scheme with fully asynchronous control is utilized as the enabling building block to meet the stringent power dissipation and efficiency requirements of this application. The resulting power electronics do not contain magnetic components and can be integrated into an LSI chip.
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1. Introduction

Extension of battery life to a full workday while preserving high mobility is a fundamental concern for Thin and Light computing platforms [1]. Critical development areas have been identified in the industry such as energy efficient cooling (the need to dissipate over 50 W in a size constrained box) [2], higher density energy sources, fast renewable sources, and enhanced power and thermal management features [3]. Much work has been done on silicon power efficiency techniques, power management features, and new costly cooling technologies. An approach that has not been thoroughly investigated is to model each platform as an isolated island where access to the resources of the "mainland" entails high cost. This dictates the effective use of energy sources in the vicinity of the computer. In a separate paper, the authors have examined fundamental issues related to the integration of thermoelectric (TE), photovoltaic (PV) and piezoelectric power modules for battery life extension in mobile computing platforms [4].

Power conversion efficiency has been identified as a significant barrier in the feasibility of the integration of these low power renewables from low, intermittent voltage levels to the system dc bus voltage required to charge a battery. This paper will present the implementation of an innovative charge pump boost converter for integration with low power renewables, resulting in enhancements to mobile power architectures for green notebook designs. At the heart of the proposed power conversion system is an asynchronous charge pump designed to achieve net battery life benefits.

2. Integrated sustainable power management

The motivation for integrating renewable sources in a mobile computing platform is a direct consequence of the current design trends in thin and light notebook systems. These can be summarized as

(i) *Longer battery life*. New technologies [1] drive energy efficient operation and longer lasting batteries.
(ii) *Performance on demand*. The performance is expected to scale up to desktop computing capabilities over time.
(iii) *Compact design*. Systems become thinner, smaller, and lighter in order to enable mobility which makes it challenging to cool high power density components.

* Corresponding author. Tel.: +1 541 737 9357; fax: +1 541 737 4600.
E-mail address: alex.yokochi@orst.edu (A. Yokochi).
[1] Present address: Department of Electrical and Electronics Engineering, Middle East Technical University, North Cyprus Campus, Turkey.

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Table 1
Current, voltage, and power range for TE and PV integration

Design range	I (mA)	V (V)	P (mW)
TE	0–50	0–0.5	0–25
PV	1–100	0.5–5	0.5–500

(iv) *Cost*. Mainstream mobile computing platforms need to be cost aware in order to enable large volumes. This requirement prevents expensive solutions from being deployed to address issues associated with (i)–(iii).

In response to (i) above, dynamic system management is necessary and common in high-performance platforms to reduce power demands, and dynamically trade off performance against power. Among the response mechanisms are voltage and frequency scaling, decode throttling, speculation control, and *I*-cache toggling. For example, the frequency and voltage scaling scheme reported in [5] yields a 50% power reduction but limits the performance impact to 20% for the duration of the event. It is expected in the future that systems will be designed to respond dynamically to the requirements of a particular application for maximum efficiency and reliability, as exemplified by fan speed control [6], and Enhanced Intel Speedstep® [7] technologies.

2.1. Use of renewables for power management

Scavenging energy from renewable sources in the vicinity of the computing system is an elegant method for saving power and thus extending battery life. The problem with small-scale renewable sources is the low efficiency associated with significantly stepping up the low-voltage output to allow integration with the system battery. In addition, there may not be any net benefit after accounting for the power dissipation in the required converter. The problem is compounded if scalability to multiple sources with different characteristics and intermittent properties are considered.

Two renewable energy sources in particular are considered viable for enhanced power management due to favorable characteristics in extracting mWatts to thousands of mWatts depending on the conditions: thermoelectric (TE) and photovoltaic (PV). Prior work has shown these to be the power sources with the highest potential benefits as determined from commercially available bulk modules [4]. As reported, the use of a readily available low cost, low efficiency PV module could extend the battery life by approximately 5%, and the use of a state-of-the-art, high efficiency, multi-junction PV module could extend the lifetime by up to 25%.

Notebook integrated TE and PV output power specifications are summarized in Table 1 per module. It can be recognized from the table that achieving the goal of net battery life benefit will require setting system ON/OFF thresholds for the low end of the power range, so that power scavenging is inactivated when power electronics consume higher power than generated power. Voltage, current, and power always scale together for TE and PV, allowing only one of these parameters (e.g. voltage) to be utilized in ON/OFF thresholds.

The two types of energy sources have different integration issues, but share the fact that depending on the operating conditions under which the mobile computing platform is used (e.g., variable CPU performance demand, variable light intensity) variable voltage levels are produced by the integrated power generation module. Specifically, low light levels will generate low power levels from PV modules, and low CPU performance demand can decrease the heat produced by the system which will, in turn, lead to low TE module voltages. A proposed system would therefore need to detect different voltage levels and dynamically scale the power electronics in order to achieve the best efficiency.

A new approach is taken in this work with the goal of making energy from renewable sources available to the mobile computing system as a means for extending battery life. This approach also advances recent industry initiatives, like Energy Star [8], to design computer platforms with environmentally friendly characteristics. Some characteristics, which ensure that mobile platforms with sustainable power management are superior to the existing systems, are identified below:

(i) *Battery life assumptions*. Longevity should be improved by providing net charge directly to the system battery instead of powering up specific sub-systems (as opposed to the implementation in [9]). The generated power should be higher than the power dissipated in the power electronics interfacing with the renewable sources for net battery life benefit. Renewable sources like PV components should be enabled to scavenge energy even when the system is off. When the system is on, the renewable power should supplement both the externally supplied ac power (e.g. from the cord connected power supply) or the dc power from the battery. This is a highly desirable attribute for a truly green implementation.
(ii) *Performance assumptions*. It is not acceptable to degrade system performance as a result of integrating renewable sources. In fact any TE component used to scavenge thermal energy should operate in hybrid mode, as discussed in [10,11], in order to offset negative performance impact from reduced cooling capacity, and even improve performance when required by the system tasks.
(iii) *Size*, *cost*, *and scalability assumptions*. The added renewable components and associated power electronics should represent common technology for lowest cost. They should be scalable with system size. Power electronics should be compact, and easy to integrate into an LSI chip. Magnetic components should therefore be minimized or avoided.

3. New sustainable power architecture

In a conventional mobile power architecture, wall ac voltage is rectified to ∼19.5 V dc, which is further stepped down by dc/dc converters for system loads, as depicted in Fig. 1. The battery charger bucks down the voltage to ∼10.8–16.8 V depending on the charge state. When unplugged, the input to the dc/dc converters switches to the battery.

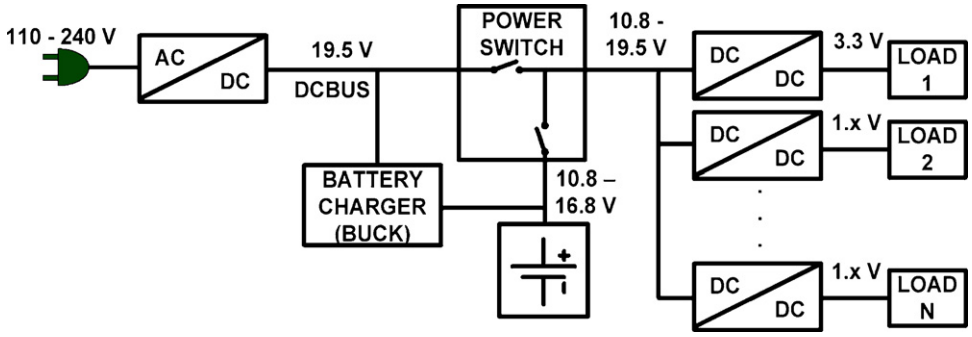

Fig. 1. Conventional notebook power architecture.

Table 2
Boost converter topology comparison summary (circuit device and capacitor sizes consistent for comparison)

First stage boost converter	Second stage boost converter	Source P (mW)	First stage gen. P (mW)	Second stage gen. P (mW)	Generation surplus (mW)	Input–output efficiency (%)
Conventional	Conventional	9.1	4.7	2.0	2.0	22
Conventional	Dickson charge pump	9.0	4.5	3.4	3.4	37
Dickson charge pump	Dickson charge pump	10.0	3.1	2.3	2.3	23
CMOS low-V charge pump	Dickson charge pump	9.4	5.5	4.1	4.1	44

Recent focus in the industry to improve cost, real estate, and efficiency has resulted in alternative architectures with lower dc Bus voltage. The first implementation in Fig. 2 (top) [12] incorporates a bi-directional buck/boost converter between the dc bus and the battery. The ac/dc converter is enhanced with logic in the second configuration (Fig. 2 (bottom)) [13]. It interfaces to the notebook to communicate power demand requirement vs. supply capability back and forth, and dynamically regulates the dc Bus voltage. The renewable energy sources must then be somehow efficiently integrated with such a system. In particular, the low voltage and power levels described in Table 1 imply that an efficient voltage boost converter needs to be integrated here.

3.1. Power gating per renewable module

Voltage boost is an inherently inefficient process, especially when large voltage multipliers are concerned. Adding to this, the low power levels available from the small-scale renewable sources, it becomes crucial for each boost module to monitor available input power and decide whether the associated power

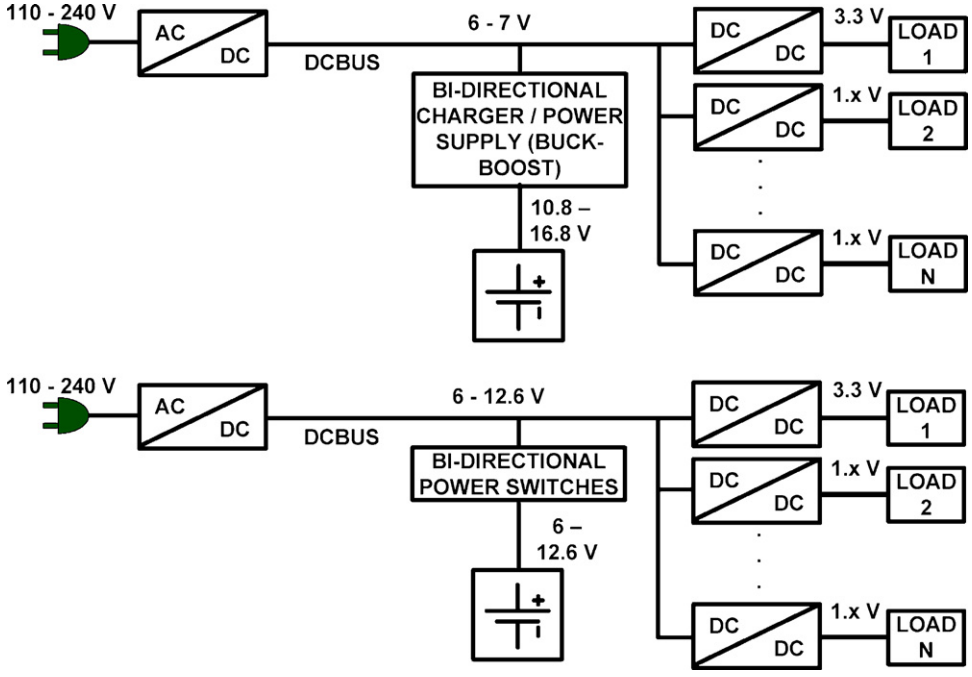

Fig. 2. Emerging architectures with low dc bus voltage: bi-directional buck/boost [12] (top), and ac/dc with adjustable output voltage (IMPAP) [13] (bottom).

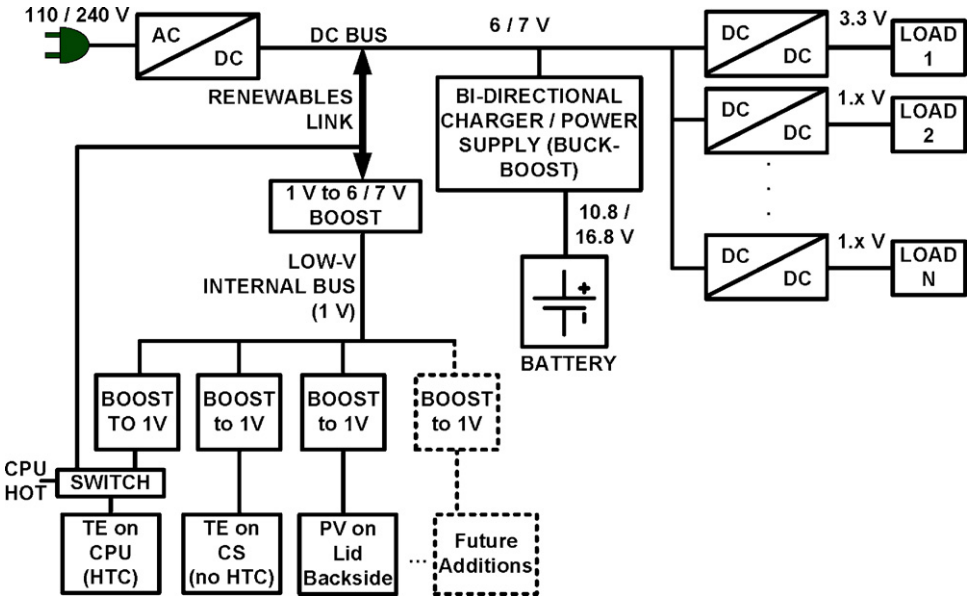

Fig. 3. New sustainable power architecture with renewables link.

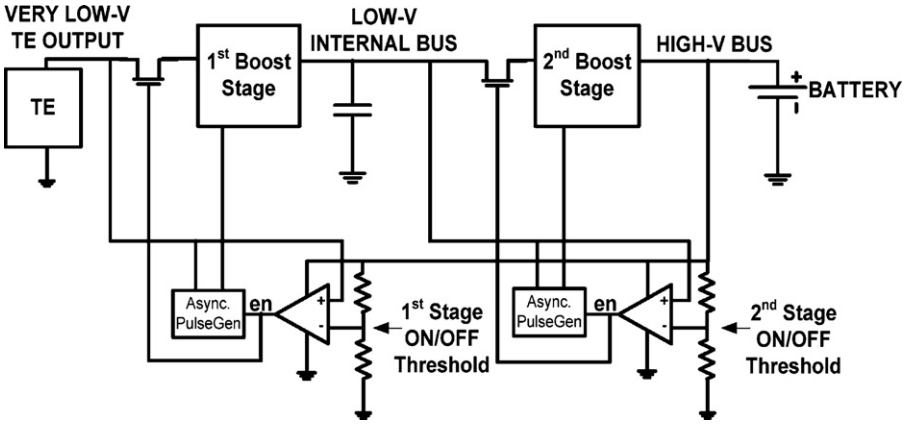

Fig. 4. Asynchronous controller topology for low power renewables applications.

electronics should be enabled. Otherwise, the sub-circuits should be power gated to avoid wasting power. For this reason, we define here two metrics to evaluate the proposed power converter designs. The utilized figures of merit for the evaluation are:

$$\text{input-to-output\_efficiency} = \frac{\text{output\_power}}{\text{total\_input\_power}} \quad (1)$$

$$\text{generation\_surplus} = \text{net\_output\_power-consumed\_PE\_power} \quad (2)$$

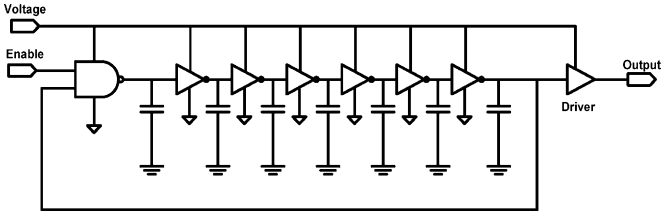

Fig. 5. Ring oscillator used as an asynchronous pulse generator with voltage controlled switching frequency and power dissipation.

Input-to-output (*I–O*) *efficiency* tracks generated power as compared to the total power from the TE module plus any additional power delivered to the power electronics. *Generation surplus* must be larger than 0 for a particular boost converter design to have net benefit. PE in the surplus equation denotes power electronics. The generation surplus is as important in sustainable power management as the I–O efficiency. In order to optimize this overall input to output power efficiency, the voltage setting at the internal bus must be optimized. An optimal voltage is likely to be such that the first stage and second stage boost multipliers are simultaneously minimized, and hence are roughly equal. This requirement drives the internal bus voltage to be 1–2 V for the TE output voltage range.

The next consideration is the topology selection and design of the boost converter for low voltage, low power sources. Clearly, power dissipation in power electronics associated with the boost converters will be most challenging for scavenging power. Three requirements have been identified for controller design in order to address this problem:

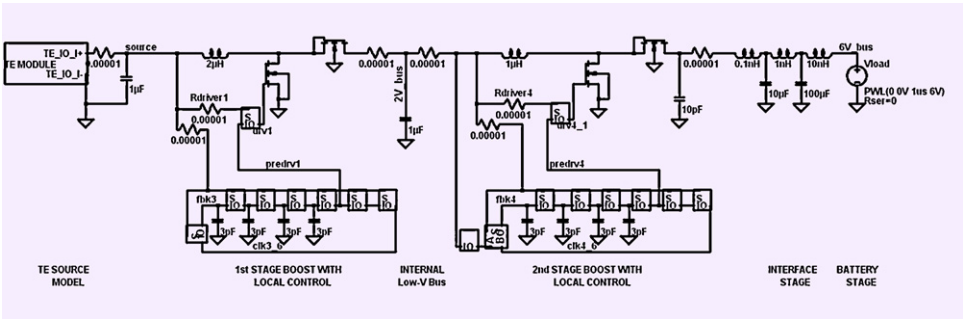

Fig. 6. Circuit simulation model in 90 nm CMOS for two stage conventional boost topology with local control.

(i) Minimize the number of power consuming transistors. Sophisticated and high device count schemes such as pulse width modulation will result in diminishing returns due to the intermittent and low power nature of the TE source.
(ii) Any boost stage should not turn on unless the corresponding control circuit will consume less power than the power generated at the stage output. The ON/OFF threshold can be determined empirically for different power sources.
(iii) The controller switching frequency and the associated power dissipation should scale down with TE power output in order to make net energy scavenging viable under low power conditions. When the minimum power generation requirement from (ii) can no longer be met, the controller should shut off (Fig. 3).

A renewables link with direct interface to the dc Bus has been added in this work. A two-stage converter is needed due to low TE voltages (Table 1). The integration of the low-voltage renewables is more viable with the emerging low-voltage dc bus architectures of Fig. 2, because they allow lower voltage boost multipliers than the conventional designs. This is an additional advantage of the emerging designs that has not been previously considered.

A controller topology resulting from these three requirements is depicted in Fig. 4. As noted in the figure, each boost stage has its own asynchronous controller unit with a minimum number of devices to satisfy requirement (i). The controller design is based on the concept of trickle-charging. First, a minimum amount of power needs to be available from the TE, as sensed through the TE output voltage. This minimum requirement is set through the resistor divider at the input of the first comparator based on requirement (ii). Once the comparator trips, the asynchronous pulse generator is enabled. The operating frequency of the pulse generator is lowest when the TE output voltage barely exceeds the ON/OFF threshold. The voltage sensing asynchronous pulse generator is implemented through a simple CMOS ring oscillator with enable input, as shown in Fig. 5.

As the voltage (and power) available from the renewable source increases, CMOS gate delay decreases and the ring oscillator operates at higher frequency with higher associated power dissipation. The pulse generator dynamic power dissipation is linearly related to the operational frequency, and has second order dependence on voltage:

$$\text{pulse generator dynamic power} = C \times \text{voltage}^2 \times f \qquad (3)$$

C in the equation denotes switching parasitic and load capacitance, and f stands for switching frequency. Controller dynamic power dissipation therefore shows a cubic dependence on TE power output, and meets requirement (iii). The only components of the controller not powered by the renewable sources are the comparator and the resistor divider for reference generation. The comparator power dissipation can be optimized since its bandwidth requirements are low. Alternatively it can be fully eliminated in an integrated solution by designing a minimum power detection capability into the pulse generator, for example using MOSFET ON threshold voltage (V_t) available from the device process technology. A low-V_t CMOS technology is required for the ring oscillator implementation in order for the controller to start pulsing at low TE output levels. Alternatively body biasing techniques [14] can be utilized to have a programmable V_t, which would in turn translate to a programmable ON/OFF threshold.

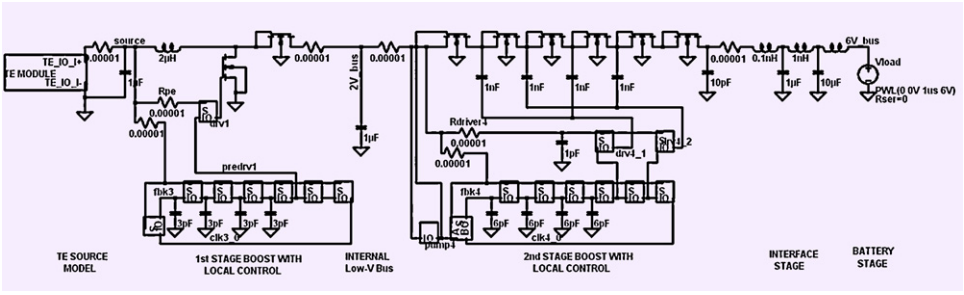

Fig. 7. Circuit simulation model in 90 nm CMOS for conventional boost and Dickson charge pump cascade.

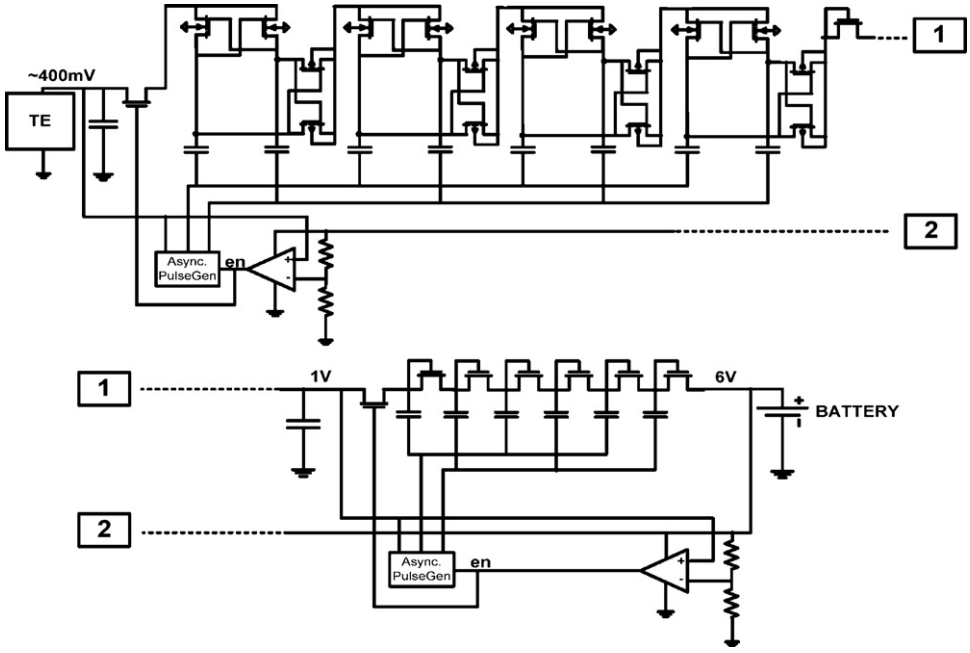

Fig. 8. Low-*V* CMOS and Dickson charge pump cascade.

Once the internal low-voltage bus becomes charged to its threshold setting, e.g. 1 V, the comparator in the 2nd controller stage (Fig. 4) trips and the pulse generator in the 2nd stage is activated. The pulses transfer the charge from the internal low-voltage bus, through the boost converter, to the high voltage bus. If the charge transfer in the 2nd stage exceeds the transfer in the 1st stage, the intermediate voltage level eventually drops and the 2nd stage controller turns off while the internal bus is recharged up to its activation level.

The controller building block is asynchronous in many ways. Control modules associated with different renewable sources can vary in switching frequencies, duty cycle, and are phase mismatched with each other. Capacitors and reference resistors shown in Figs. 4 and 5 can all be built using devices in a fully integrated CMOS design. Programmability can be added to the resistor dividers to tune ON/OFF threshold settings during system design. Similarly, the oscillator load capacitors in Fig. 5 can be designed to be programmable to allow base frequency adjustments.

3.2. Two stage conventional boost

The simulated circuit is depicted in Fig. 6. The boost converter works in discontinuous conduction mode, and the asynchronous pulse generator functions as described in the previous section. The comparator in the first stage has been eliminated, which allows first stage boost to operate as soon as the devices that make up the ring oscillator come out of the cut-off region and turn on. The active components of the circuit are implemented using 90 nm CMOS technology. The diodes are implemented as diode connected MOSFETs. The advantage of the conventional boost is its relatively simple design that is well understood. However, it has significant drawbacks including low I–O efficiency for high voltage multipliers and the required inductors that are hard to integrate. Though a positive generation surplus is achieved, poor I–O efficiency is found due to significant losses in both the 1st and 2nd stages, as shown in the first row of Table 2.

3.3. Conventional boost and Dickson charge pump cascade

Charge pumps have evolved in the recent years especially due to the integration of on-chip circuits that require higher voltage levels than available through the power supply [15]. Since the 2nd stage losses are higher than 50% in the conventional implementation of previous section, this portion of the cascade is replaced by the simplest Dickson-style charge pump [16] as depicted in Fig. 7 for comparison. The charge pump, having no inductors, significantly reduces the losses in the second stage (Table 2, 2nd row), and significantly improves both generation

Table 3
Measured TE generation efficiency comparison across main boost schemes and supply voltage levels

First stage boost converter	Second stage boost converter	Source *P* (mW)	Output power (mW)	PE consumed power (mW)	Generation surplus (mW)	Input–output efficiency (%)
Conventional (6 V)	Conventional (6 V)	0.3	0.1	7.2	−7.1	1
Dickson charge pump (6 V)	Dickson charge pump (6 V)	8.8	26.4	75.6	−49.2	26
Dickson charge pump (1 V)	Dickson charge pump (1 V)	4.5	8.0	6.0	2.0	57

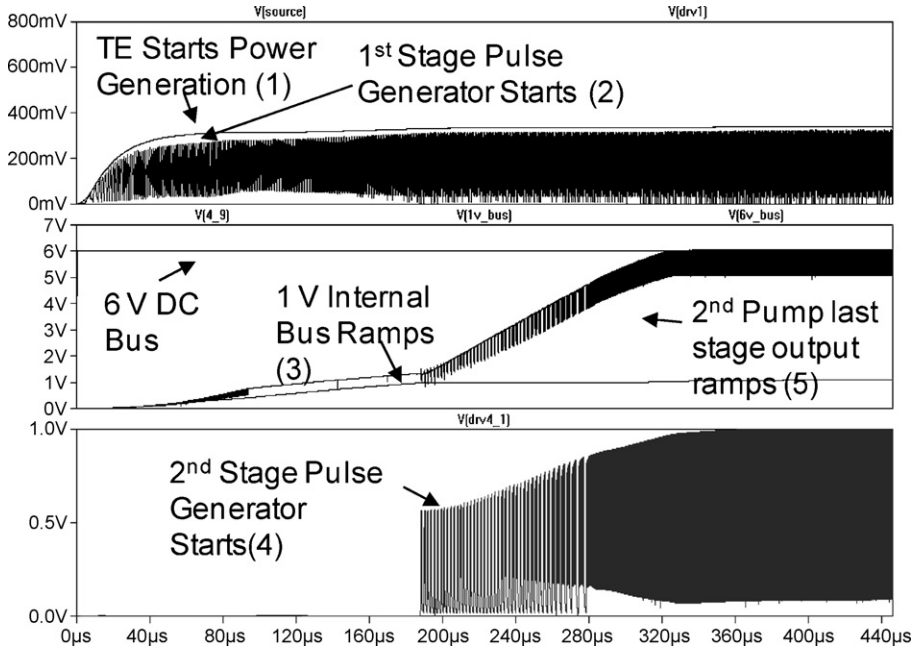

Fig. 9. Cascade charge pump startup sequence simulation.

surplus and I–O efficiency. Note that in the charge pump implementation two control pulses with opposite polarity are required. This is achieved by tapping off outputs from the last two stages of the ring oscillator in Fig. 5.

3.4. Two stage Dickson charge pump

The problem with the previous two implementations is the inductor that is hard to integrate into a CMOS LSI design. The next logical configuration to study is therefore a two stage Dickson charge pump circuit. This effectively duplicates the second stage in Fig. 7 to the first stage with some adjustments to intentional capacitance and number of stages. The voltage swing at each stage of a Dickson charge pump is

$$\Delta V = V_{\mathrm{CLK}} \frac{C}{C + C_{\mathrm{S}}} - \frac{I_{\mathrm{O}}}{f(C + C_{\mathrm{S}})} \sim V_{\mathrm{CLK}} \tag{4}$$

where V_{CLK} is control clock voltage amplitude, C is intentional capacitor per stage, C_{S} is the parasitic capacitance per stage, I_{O} is output current, and f is the effective switching frequency of the control clock. The full term can be approximated as V_{CLK}, as shown in the equation, when C is significantly larger than C_{S} and I_{O} is small. Voltage gain at stage N is

$$\mathrm{gain} = \Delta V - V_{\mathrm{th}}(N) \tag{5}$$

where $V_{\mathrm{th}}(N)$ is the MOSFET threshold voltage at stage N, and is also the voltage difference between the source and the drain. Therefore, for the T stage Dickson charge pump, the output voltage is

$$V_{\mathrm{out}} = \sum_{N=1}^{T} (V_{\mathrm{in}} - V_{\mathrm{th}}(N)) \tag{6}$$

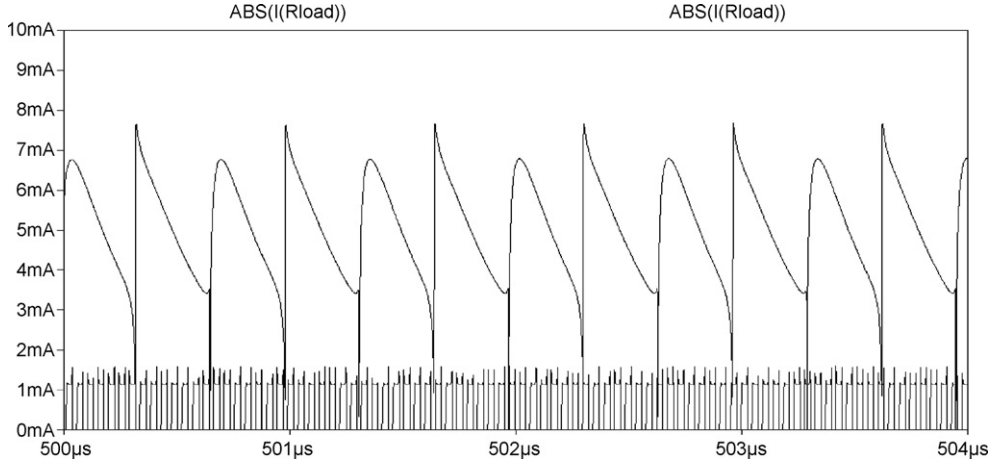

Fig. 10. 1st and 2nd stage current waveforms.

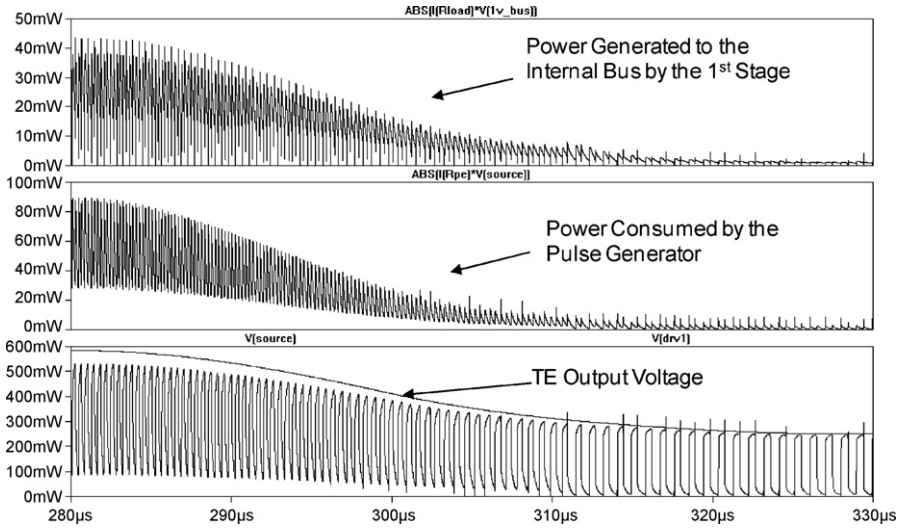

Fig. 11. TE voltage change (bottom) resulting in frequency & amplitude modulation of the control pulse (bottom), power reduction in PE (middle), and reduced generation to the internal bus (top).

With ground body bias, source to bulk voltage increases at later stages of the Dickson charge pump, which in turn increases V_{th} and diminishes returns for the added stages. Furthermore, when V_{in} is used to power up the pulse generator driving the charge pump, V_{CLK}–V_{in}, and ΔV is small at the first stage. Therefore, Dickson charge pumping gain significantly reduces, and impacts the I–O efficiency of the first stage as shown in Table 2, row 3. The low efficiency of the first stage thus reduces the overall generation surplus and IO efficiency.

3.5. Low-V CMOS and Dickson charge pump cascade

A more suitable charge pump for the first stage is the low-voltage CMOS implementation recently reported in [17]. This implementation is based on a cross-connected NMOS input pair followed by a PMOS output pair to ensure a voltage step-up by $V = V_{in}$ at each stage. The complete topology, with the low transistor count Dickson charge-pump kept at the second stage, is shown in Fig. 8.

The details of the low-voltage CMOS operation will not be described here and can be found in [17]. It should suffice to note that for the 4 stage charge pump shown in the figure, the ideal output voltage is $5(N+1)$ times V_{in}. Therefore, with the internal bus voltage set at 1 V, a V_{in} level as low as 200–250 mV should be supported by the four stages, including parasitic losses. Simulation results (Table 2, row 4) using 90 nm devices confirm that low-V and Dickson cascade is superior in generation surplus and I–O efficiency to the previous topologies.

Fig. 9 depicts the start up sequence for the cascade charge pump. TE power generation due to thermal changes is likely to ramp up much slower than what is shown, but has been shortened for simulation purposes. After sufficient power availability is detected at the TE, the pulse generator at the 1st stage starts pumping power to the internal bus as shown. The pulse generator at the 2nd stage starts when internal bus reaches 1 V, and pumps power to the dc bus.

As shown in Fig. 10, low-V CMOS and Dickson charge pumps have different output current characteristics. The Low-V CMOS at the first stage does not have dead time between

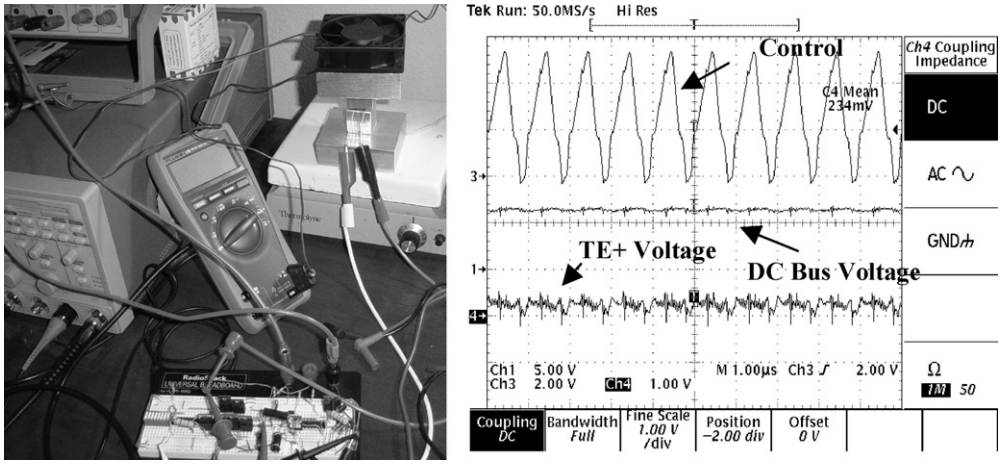

Fig. 12. TE generation prototype (left) and a subset of signals captured (right).

current pulses, because it effectively has two parallel paths pumping charge out with a 180° phase shift. On the other hand, a conventional Dickson charge pump at the 2nd stage only pumps the charge out 50% of the time.

Finally, the asynchronous pulse generator output frequency, amplitude, and power modulation with available TE voltage is depicted in Fig. 11. Since the TE output power and voltage are highly correlated, the power and performance of the power electronics scale with the available TE power as intended.

4. Proof of concept using discrete components

Before going through the cumbersome effort of fully integrated 90 nm implementation, a proof of concept was developed using discrete components in order to validate the fundamental trends and conclusions from the simulations. Ring oscillator based control was not feasible without the small-scale (e.g. 90 nm) integration. Therefore, a combination of a comparator (LM339) and a timer (LM555) with enable function controlled by the comparator were utilized to generate the equivalent of circuit in Fig. 5 for each stage. The TE generation prototype system and few sample waveforms are depicted in Fig. 12.

Two boost schemes, conventional and charge pump based, were compared for low-voltage performance. 1uH inductors, 1 uF capacitors were used together with 1N5817 Schottky diodes, and available IRF510 MOSFET switches to build the conventional topology. A Dickson charge pump was designed for both 1st and 2nd stage using 1N5817 Schottky diodes and discrete capacitors. Table 3 contains measurement results for both boost schemes. In general the efficiency improvement going from the conventional boost to the low-voltage charge pump configuration is consistent with the expectations from simulation studies. On the other hand, generation surplus can clearly be further improved by reduction of power consumed by the power electronics (PE) through integration.

5. Conclusions

A significant breakthrough in mobile computing power management will be the widespread use of renewables to scavenge energy in the immediate vicinity of the machine, such as through the use of intermittent thermoelectric (TE) and small-scale photovoltaic (PV) sources. One of the fundamental challenges in generating small amounts of power from these resources, however, has been the power conversion efficiency. The problem is compounded by the large conversion multipliers required to step up voltage, and store extracted power in the mobile computer battery.

In this work the authors have developed a mobile platform power architecture enhanced with a link suitable for the incorporation of low voltage, low power renewables, which funnels energy from various sources to the main dc bus either for storage to the battery, or for reducing electrical costs from ac. The problem of power dissipation in power electronics was addressed through a new asynchronous control scheme based on voltage sensing ring oscillators. A cascade charge pump based boost design was adopted for stepping up voltage from renewables in two stages. The low-voltage CMOS charge pump stage directly interfaces the renewable components, and is suitable for operating at very low-voltage levels as recently reported in the literature. The second stage utilizes a simple Dickson charge pump. It has been demonstrated through setup using discrete components that both the asynchronous control and the cascade charge pump topology work well for the intended application. Integration using 90 nm process or smaller is expected to improve the observed results by providing further improvements in the generation surplus metric.

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